Hall Ticket No: | | | | | | | | | | |

**Question Paper Code: 25MBVESTC01**

# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

## M.Tech. I Year I Semester (R25) Regular End Semester Examinations - January 2026

## CMOS DIGITAL IC DESIGN

(VLSI Design and Embedded Systems)

**Time: 3Hrs** **Max Marks: 100**

Attempt all the questions. All parts of the question must be answered in one place only.
**In Q.no 1 to 5 answer either A or B only**

| Q.No. | | Question | Marks | CO | BL |
|---|---|---|---|---|---|
| Q.1(A) | i | Explain the VTC characteristics of a CMOS inverter with a neat diagram. | 10M | 1 | 2 |
| | ii | Outline about $V_T$ and its dependency on various parameters. | 10M | 1 | 2 |
| | | **OR** | | | |
| Q.1(B) | i | Summarize Pseudo NMOS Logic inverter. List the drawbacks of Pseudo NMOS Logic over CMOS logic. | 10M | 1 | 2 |
| | ii | Perform the Rise time and Fall time analysis of Pseudo NMOS logic with an example. | 10M | 1 | 2 |
| Q.2(A) | i | Design one-bit full adder using CMOS logic and explain its working. | 10M | 2 | 3 |
| | ii | Explain the propagation delay and power consumption issues of CMOS gate. | 10M | 2 | 2 |
| | | **OR** | | | |
| Q.2(B) | i | Design CMOS NOR2 and NAND2 gate with the aid of necessary expressions. | 10M | 2 | 3 |
| | ii | Explain how Boolean expressions are realized using NMOS and CMOS logic gates with an example. | 10M | 2 | 2 |
| Q.3(A) | i | Distinguish between flip-flops and latches. | 10M | 3 | 3 |
| | ii | Explain the behaviour of bistable elements with suitable waveforms. | 10M | 3 | 3 |
| | | **OR** | | | |
| Q.3(B) | i | Outline about the edge triggered D flip-flop using CMOS logic. | 10M | 3 | 3 |
| | ii | Explain about setup time, hold time, and clock skew in sequential circuits. | 10M | 3 | 2 |
| Q.4(A) | i | Analyze about voltage bootstrapping with an example. | 10M | 4 | 4 |
| | ii | Explain the speed and power dissipation in dynamic CMOS logic. | 10M | 4 | 2 |
| | | **OR** | | | |
| Q.4(B) | i | Outline about High performance Dynamic CMOS circuits. | 10M | 4 | 2 |
| | ii | Explain the speed and power dissipation in dynamic CMOS logic. | 10M | 4 | 2 |
| Q.5(A) | i | Distinguish between SRAM and DRAM cells. | 10M | 5 | 3 |
| | ii | Explain the principle of NAND gate flash memory with a neat diagram. | 10M | 5 | 2 |
| | | **OR** | | | |
| Q.5(B) | i | Classify semiconductor memories and explain their characteristics. | 10M | 5 | 2 |
| | ii | Explain the SRAM cell operation with a diagram. | 10M | 5 | 2 |

***END***

Hall Ticket No: | | | | | | | | | | |

**Question Paper Code: 25MBVESTC02**

# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

## M.Tech. I Year I Semester (R25) Regular End Semester Examinations - January 2026

## ADVANCED MICROCONTROLLERS AND SIGNAL PROCESSORS

(VLSI Design and Embedded Systems)

**Time: 3Hrs** **Max Marks: 100**

Attempt all the questions. All parts of the question must be answered in one place only.
**In Q.no 1 to 5 answer either A or B only**

| Q.No. | Question | Marks | CO | BL |
|---|---|---|---|---|
| Q.1(A) | Analyse the Cortex-Mx programming model by examining the role of special registers (PSP, MSP, CONTROL, PRIMASK) in handling real-time application requirements | 20 | 1 | 4 |
| | **OR** | | | |
| Q.1(B) | Analyse the internal bus interface and instruction pipeline of Cortex-Mx and explain how they enhance processor performance. | 20 | 1 | 4 |
| Q.2(A) | Explain Nested Vectored Interrupt Controller (NVIC) structure and describe key registers involved in interrupt prioritisation. | 20 | 2 | 2 |
| Q.2(B) | Explain SysTick timer architecture, its configuration registers, and role in generating periodic interrupts for embedded timing applications | 20 | 2 | 2 |
| Q.3(A) | Analyse GPIO pin multiplexing and fast I/O architecture in LPC 17xx and discuss application relevance. | 20 | 3 | 4 |
| | **OR** | | | |
| Q.3(B) | Analyse power management features in LPC 17xx microcontroller and evaluate their significance in low-power embedded designs. | 20 | 3 | 4 |
| Q.4(A) | Apply the DSP processor architecture to illustrate signal flow through MAC unit during filtering operation. | 20 | 4 | 3 |
| | **OR** | | | |
| Q.4(B) | Apply DSP addressing techniques to illustrate the role of modulo addressing in convolution and FIR filter processes | 20 | 4 | 3 |
| Q.5(A) | Examine the addressing modes and execution characteristics of TMS320C55x DSP processors. | 20 | 5 | 4 |
| | **OR** | | | |
| Q.5(B) | Analyse pipeline depth, functional units and delay slot behaviour in VLIW-based TI DSP architectures. | 20 | 5 | 4 |

***END***

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBCOMTC01

# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

## M.Tech. I Year I Semester (R25) Regular End Semester Examinations - January 2026

## RESEARCH METHODOLOGY AND IPR

(Common to CSE and VES)

**Time: 3Hrs** **Max Marks: 100**

Attempt all the questions. All parts of the question must be answered in one place only.
**In Q.no 1 to 5 answer either A or B only**

| Q.No. | | Question | Marks | CO | BL |
|---|---|---|---|---|---|
| Q.1(A) | | Define research and discuss its importance in the contemporary world. Describe the research process in detail, illustrating the various stages with a suitable diagram. | 20 | 1 | 2 |
| | | **OR** | | | |
| Q.1(B) | | Discuss the importance of critical literature review and its uses in planning innovation research. | 20 | 1 | 2 |
| Q.2(A) | | What do you mean by "Sample Design"? Under what circumstances one should use a probability sample? | 20 | 2 | 2 |
| | | **OR** | | | |
| Q.2(B) | | List the different methods of collecting data. Explain the observation method of collecting data with its merits and demerits. | 20 | 2 | 2 |
| Q.3(A) | i | What is oral presentation? What are merits and demerits of oral presentation? | 10 | 3 | 2 |
| | ii | What are the items in a research report? Explain them in brief. | 10 | 3 | 2 |
| | | **OR** | | | |
| Q.3(B) | | Describe the process of formulating a research hypothesis. Explain the objectives and significance of hypothesis formulation in research. | 20 | 3 | 2 |
| Q.4(A) | i | Define trade secrets and discuss their protection mechanisms. | 10 | 4 | 2 |
| | ii | Write a short note to summarize the all types of intellectual property rights. | 10 | 4 | 2 |
| | | **OR** | | | |
| Q.4(B) | | Discuss the relationship between IPR and biodiversity, including relevant international agreements. | 20 | 4 | 2 |
| Q.5(A) | | What are the choices for patent application to be filed? Mention the patent application forms & explain the concept of 'claims. | 20 | 5 | 2 |
| | | **OR** | | | |
| Q.5(B) | | Explain the examination and grant process of a patent. What are the different types of patent revocation? | 20 | 5 | 2 |

***END***

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESDC03

# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

## M.Tech. I Year I Semester (R25) Regular End Semester Examinations - January 2026

## FPGA ARCHITECTURES AND APPLICATIONS

(VLSI Design and Embedded Systems)

**Time: 3Hrs** **Max Marks: 100**

Attempt all the questions. All parts of the question must be answered in one place only.
**In Q.no 1 to 5 answer either A or B only**

| Q.No. | | Question | Marks | CO | BL |
|---|---|---|---|---|---|
| Q.1(A) | i. | Describe Complex Programmable Logic Devices (CPLDs) with reference to the Xilinx CoolRunner XCR3064XL CPLD. | 10 | 1 | 3 |
| | ii. | Explain its architecture and demonstrate the implementation of a parallel adder with accumulation using CPLD. | 10 | | |
| | | **OR** | | | |
| Q.1(B) | i. | Explain about PROM and implement: f1 = Σ (0, 1, 2, 3, 4, 6, 8) and f2 = Σ (0, 2, 3, 4, 5). | 15 | 1 | 3 |
| | ii. | Write the differences between CPLD and FPGA. | 5 | | |
| Q.2(A) | | Explain in detail about FPGA based system design with proper diagram | 20 | 2 | 2 |
| | | **OR** | | | |
| Q.2(B) | i. | What are the various programmable technologies of FPGA? | 10 | 2 | 2 |
| | ii. | Explain each methodology with neat diagram | 10 | | |
| Q.3(A) | i. | Explain SRAM-based FPGA programming technology. | 10 | 3 | 2 |
| | ii. | Describe the device architecture of SRAM programmable FPGAs, highlighting advantages and limitations. | 10 | | |
| | | **OR** | | | |
| Q.3(B) | | Explain about FPGA design flow with proper flow chart. | 20 | 3 | 2 |
| Q.4(A) | i. | Explain about 4 bit counter Macro | 10 | 4 | 3 |
| | ii. | Explain Cascade multiplexer Macro | 10 | | |
| | | **OR** | | | |
| Q.4(B) | i. | Explain about ACT3 combinational and sequential module. | 10 | 4 | 2 |
| | ii. | Explain about antifuse networking | 10 | | |
| Q.5(A) | | Explain about ACT 1 5 bit binary counter with proper circuit diagram | 20 | 5 | 2 |
| | | **OR** | | | |
| Q.5(B) | i. | Explain the concept of position tracking for a robot manipulator in controlling a high precision robot with 16 degrees of freedom. | 10 | 5 | 2 |
| | ii | With the help of diagram explain the architecture of high-speed DMA controller. | 10 | | |

***END***

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESDC04

# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

## M.Tech. I Year I Semester (R25) Regular End Semester Examinations - January 2026

## LOW POWER VLSI DESIGN

(VLSI Design and Embedded Systems)

**Time: 3Hrs** **Max Marks: 100**

Attempt all the questions. All parts of the question must be answered in one place only.
**In Q.no 1 to 5 answer either A or B only**

| Q.No. | | Question | Marks | CO | BL |
|---|---|---|---|---|---|
| Q.1(A) | i | Describe the need for low power VLSI design by discussing its impact on battery operated and high-density integrated circuits. | 10 | 1 | 2 |
| | ii | Discuss the causes of surface scattering and velocity saturation in MOSFETs and explain how it can be minimized in modern devices | 10 | 1 | 2 |
| | | **OR** | | | |
| Q.1(B) | i | Discuss Drain Induced Barrier Lowering and Punch Through effects in short channel MOSFETs? | 10 | 1 | 2 |
| | ii | Explain the concept of Short Circuit power dissipation? | 10 | 1 | 2 |
| Q.2(A) | i | Examine suitable techniques to explain how switched capacitance can be minimized. | 10 | 2 | 4 |
| | ii | Demonstrate any four voltage scaling techniques in reducing power consumption and discuss their impact on circuit performance. | 10 | 2 | 3 |
| | | **OR** | | | |
| Q.2(B) | i | Distinguish between VTCMOS and MTCMOS for leakage power reduction. | 10 | 2 | 3 |
| | ii | Apply the concepts of pipelining and parallel processing to improve the performance of digital systems and illustrate with suitable examples. | 10 | 2 | 4 |
| Q.3(A) | i | Design a CMOS Full Adder and discuss its performance. | 10 | 3 | 4 |
| | ii | Design a Carry Save Adder and explain with an example. | 10 | 3 | 4 |
| | | **OR** | | | |
| Q.3(B) | | Derive the carry equations for a 4-bit Carry Look-Ahead Adder and analyze how parallel carry computation improves speed. | 20 | 3 | 4 |
| Q.4(A) | i | Illustrate different types of multiplier architectures and explain | 10 | 4 | 4 |
| | ii | Design a 4x4 bit Braun Array Multiplier to multiply two unsigned binary numbers and explain with an example. | 10 | 4 | 4 |
| | | **OR** | | | |
| Q.4(B) | i | Design the Baugh Wooley multiplier and explain its operation with its algorithm. | 20 | 4 | 4 |
| Q.5(A) | i | Analyze low-power SRAM technologies with neat diagrams. | 10 | 5 | 4 |
| | ii | Illustrate the basic architecture of a 6T SRAM with a neat diagram and explain its operation. | 10 | 5 | 4 |
| | | **OR** | | | |

| | | | | | |
|---|---|---|---|---|---|
| **Q.5(B)** | i | Investigate the future trends and developments in ROM technology and their impact on modern memory systems. | 10 | 5 | 4 |
| | ii | Draw 4 bit X 4 bit NAND based ROM array and explain with look up table. | 10 | 5 | 4 |

*****END*****